in the NFET region **100** constitutes a chemical oxide portion **50'**. The second doped semiconductor portion **60**A, the metal gate portion **54'**, the high-k material portion **52'**, and the chemical oxide portion **50'** collectively constitute a first gate stack structure.

[0060] Referring to FIG. **13**, the fifth photoresist **67** is removed, for example, by ashing. The exposed surfaces of the exemplary semiconductor structure may be cleaned at this step.

[0061] Referring to FIG. **14**, the first dielectric gate cap **62**A and the second dielectric gate cap **62**B are removed, for example, by a wet etch selective to the first gate stack structure (**50'**, **52'**, **54'**, **60**A) and the second gate stack structure (**40'**, **44'**, **60**B). Preferably, the wet etch is selective to the shallow trench isolation structure **20** and the substrate semiconductor layer **10**. For example, the first and second dielectric gate caps (**62**A, **62**B) may comprise silicon nitride and the wet etch may employ a hot phosphoric acid that removes silicon nitride selective to silicon, silicon oxide, and metal.

[0062] Referring to FIG. **15**, an oxygen-impermeable dielectric layer **70** is formed directly on the first gate stack structure (**50'**, **52'**, **54'**, **60**A) and the second gate stack structure (**40'**, **44'**, **60**B), for example, by chemical vapor deposition such as LPCVD, RTCVD, PECVD, etc. The oxygen-impermeable dielectric layer **70** comprises a dielectric material that blocks diffusion of oxygen, i.e., is impermeable for the purpose of through-diffusion of oxygen. An exemplary material for the oxygen-impermeable dielectric layer **70** includes a dielectric nitride such as silicon nitride. The oxygen-impermeable dielectric layer **70** laterally abuts the sidewalls and a top surface of the first gate stack structure (**50'**, **52'**, **54'**, **60**A) and sidewalls and a top surface of the second gate stack structure (**40'**, **44'**, **60**B) as well as exposed top surfaces of the semiconductor substrate **8**. The thickness of the oxygen-impermeable dielectric layer **70** may be from about 4 nm to about 80 nm, and preferably from about 10 nm to about 40 nm, although lesser and greater thicknesses are also contemplated herein.

[0063] Referring to FIG. **16**, a sixth photoresist **77** is applied over the oxygen-impermeable dielectric layer **70** and lithographically patterned to exposed the portion of the oxygen-impermeable dielectric layer **70** in the PFET region **200**, while covering the portion of the oxygen-impermeable dielectric layer **70** in the NFET region **100**. The exposed portion of the oxygen-impermeable dielectric layer **70** is subsequently etched by a wet etch or a dry etch. Preferably, the etch is selective to the substrate semiconductor layer **10** and the shallow trench isolation structure **20**. In case the oxygen-impermeable dielectric layer **70** comprises silicon nitride, a wet etch chemistry including hydrofluoric acid (HF) and ethylene glycol (EG) or a dry etch chemistry employing CHF_3 may be employed.

[0064] Referring to FIG. **17**, the sixth photoresist **77** is removed, for example, by ashing. Exposed surfaces of the exemplary semiconductor structure may be cleaned at this step.

[0065] Referring to FIG. **18**, a low dielectric constant (low-k) material layer (not shown) is deposited by a conformal deposition such as low pressure chemical vapor deposition (LPCVD) or rapid thermal chemical vapor deposition (RTCVD). An anisotropic etch is performed on the low-k material layer to remove horizontal portions of the low-k material layer and to form spacers from vertical portions of the low-k material layer. Remaining portions of the low-k material layer on the sidewalls of the oxygen impermeable dielectric layer **70** and on the sidewalls of the second gate stack structure (**40'**, **44'**, **60**B) respectively constitute a first low dielectric constant (low-k) gate spacer **80**A and a second low-k gate spacer **80**B.

[0066] Both the first low-k gate spacer **80**A and the second low-k gate spacer **80** B comprise a dielectric material having a dielectric constant less than 4.0. The first and second low-k gate spacers (**80**A, **80**B) may comprise silicon oxide having a dielectric constant of about 3.9. Alternately, the first and second low-k gate spacers (**80**A, **80**B) may comprise a low-k dielectric material having a dielectric constant less than 2.8. The low-k dielectric material may be porous or non-porous, and may be a spin-on low-k dielectric material such as thermosetting polyarylene ether or an organosilicate glass that is formed by chemical vapor deposition (CVD). The widths of the first low-k gate spacer **80**A and the second low-k gate spacer **80**B, as measured laterally at the bottom of each, may be from about 10 nm to about 100 nm, and typically from about 15 nm to about 60 nm.

[0067] Referring to FIG. **19**, horizontal portions of the oxygen-impermeable dielectric layer **70** is removed by an etch, which may be a wet etch or a dry etch. The remaining portion of the oxygen-impermeable dielectric layer **70** between the first gate stack structure (**50'**, **52'**, **54'**, **60**A) and the first low-k spacer **80**A constitutes an oxygen-impermeable dielectric spacer **70'**. The oxygen-impermeable dielectric spacer **70'** has an L-shaped vertical cross-sectional area, laterally abuts the first gate stack structure (**50'**, **52'**, **54'**, **60**A), and vertically abuts the substrate semiconductor layer **10**.

[0068] On one hand, diffusion of oxygen or other gas molecules into the high-k material portion **54'** during subsequent processing steps is prevented by the oxygen-impermeable dielectric spacer **70'**, thus keeping the composition of the high-k material portion **54'** constant. Particularly, the material of the high-k material portion **54'** is not subjected to further oxidation during subsequent processing steps. Thus, the high-k material portion **54'**, which is the gate dielectric material of the first gate stack structure (**50'**, **52'**, **54'**, **60**A), maintains constant composition.

[0069] On the other hand, the second low-k spacer **80**B laterally abuts the second gate stack structure (**40'**, **44'**, **60**B), providing a lower parasitic capacitance between the gate electrode, which comprises the first doped semiconductor portion **44'** and the third doped semiconductor portion **60**B, and the substrate semiconductor layer **10**. Such reduction in the parasitic capacitance contributes to enhanced performance of a transistor comprising the second gate stack structure (**40'**, **44'**, **60**B) by allowing a faster operation of the transistor compared to a transistor having the same second gate structure (**40'**, **44'**, **60**B) and a gate spacer that comprises an oxygen-impermeable dielectric material such as silicon nitride, which has a dielectric constant of about 7.5 and consequently a higher parasitic capacitance.

[0070] While the present invention has been particularly shown and described with respect to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in forms and details may be made without departing from the spirit and scope of the present invention. It is therefore intended that the present invention not be limited to the exact forms and details described and illustrated, but fall within the scope of the appended claims.